ABSTRACT

[33] Systems and methods for creating a limited duration clock divider reset are disclosed. Aspects of the invention may include a method for resetting a chip or a circuit. The method may include buffering a main reset input signal, inverting the main reset input signal to create an active high reset signal, resetting a counter utilizing the active high reset signal, comparing a counter output value and a counter-associated value in a comparator to obtain a comparator output value, and applying an OR logical operation to the comparator output. A limited duration clock divider reset may be generated from the output of the OR logical operation. The OR logical operation may be applied to the buffered main reset input signal. The comparator output may be inverted.